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evidence. See generally *Calvin Klein*, 815 F.2d at 504-05.

III.

[1] The district court's judgment denying plaintiff's request for preliminary relief is affirmed. Plaintiff's right to injunctive relief must be determined after a trial in which plaintiff is able to present all relevant evidence for the court's consideration. Each party shall bear its own costs in this appeal.

Court of Appeals, Federal Circuit

Intel Corp. v. International Trade Commission

Nos. 89-1534, 89-1459, 89-1476

Decided September 17, 1991

PATENTS

1. Infringement — Defenses — License (§120.1102)

Title — Construction of license agreement (§150.07)

License between patent holder and manufacturer does not provide patent infringement defense for Tariff Act respondent that purchased allegedly infringing products from manufacturer and resold them as its own products, since there is no evidence that parties intended license agreement to permit manufacturer to act as "foundry" for any third party who wishes to manufacture products utilizing licensor's patents, rather than to restrict scope of license to products designed and made by manufacturer itself, and since latter, narrow construction of license is consistent with other provisions of agreement.

JUDICIAL PRACTICE AND PROCEDURE

2. Procedure — Judicial review — Standard of review — Patents (§410.4607.09)

Whether particular activity raises on-sale bar of 35 USC 102(b) is question of law, based on underlying factual considerations.

PATENTS

3. Patentability/Validity — Anticipation — Prior sale — "Sale" (§115.0707.03)

International Trade Commission did not err by refusing to find that Tariff Act complainant's patent was invalid under on-sale bar of 35 USC 102(b), even though record shows that claimed invention was reduced to practice prior to critical date, that complainant gave products embodying invention to its salespersons prior to critical date, that salespersons were expected to distribute these samples to their customers, and that complainant was seeking commercial advantage by such distribution, since respondent offered no evidence that complainant actually made sales or offers to sell prior to critical date, and conclusion that offers or sales would have been "likely" under such circumstances does not constitute clear and convinc-

ing evidence required for finding of invalidity.

4. U.S. International Trade Commission — Appeals (§155.09)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Judicial review — Standard of review — Patents (§410.4607.09)

Finding of infringement under doctrine of equivalents is factual determination, and factual findings of International Trade Commission are reviewed under substantial evidence standard on appeal.

PATENTS

5. Infringement — Doctrine of equivalents — In general (§120.0701)

International Trade Commission properly held that accused erasable programmable read-only memories infringed complainant's patent under doctrine of equivalents, since hearing testimony fully supported findings that multiplexer of accused EPROMs performed selective signal acceptance function of address buffer claimed in patent and that even though multiplexer itself did not act as buffer, that function was performed elsewhere in accused devices, and since it thus cannot be held that infringement findings were unsupported by substantial evidence.

6. Infringement — In general (§120.01)

Showing that accused erasable programmable read-only memories are not intended to perform "page mode" addressing does not preclude finding that accused EPROMs infringe patented EPROM under doctrine of equivalents, since direct infringement, as opposed to induced and contributory infringement, does not require showing of intent, and therefore accused EPROMs need only be capable of operating in "page mode" to be infringing.

7. Infringement — Doctrine of equivalents — In general (§120.0701)

U.S. International Trade Commission — Procedure (§155.02)

Expert witnesses' failure to state their opinions in terms of established three-part test for infringement under doctrine of equivalents does not warrant reversal of International Trade Commission's finding of infringement under that doctrine, since commission resolves patent infringement disputes with some regularity and thus is aware of doctrine of equivalents jurisprudence,

since commission demonstrated its awareness of three-part test and applied it to facts, and since expert testimony, although not given in precise function/way/result terminology, fully supports commission's analysis.

8. Patentability/Validity — Obviousness — In general (§115.0901)

U.S. International Trade Commission — Appeals (§155.09)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Judicial review — Standard of review — Patents (§410.4607.09)

Obviousness is question of law based on series of factual determinations, including scope and content of prior art, differences between art and claims at issue, level of ordinary skill in art, and any other objective evidence; factual determinations underlying International Trade Commission's finding of non-obviousness are reviewed under substantial evidence standard, but holding of non-obviousness itself is reviewed *de novo*.

PATENTS

9. Patentability/Validity — Obviousness — Relevant prior art — Particular inventions (§115.0903.03)

Patentability/Validity — Obviousness — Secondary considerations generally (§115.0907)

International Trade Commission correctly determined that respondents to Tariff Act complaint failed to prove that complainant's patent was invalid for obviousness, even though patent, which employs extended side walls to shield electrically programmable read-only memory cells from erasure by ultraviolet radiation, appears to embody only minor advance over prior art, since extension of sidewalls increased life of EPROM cells demonstrably, giving them previously unknown practical uses, since evidence shows that sidewall extensions produced surprising results, and since respondents themselves attempted but failed to design unerasable cells.

JUDICIAL PRACTICE AND PROCEDURE

10. Procedure — Judicial review — Standard of review — Patents (§410.4607.09)

Claim interpretation is question of law subject to *de novo* review on appeal; claims are to be interpreted in light of claim lan-

guage, specification and prosecution history of patent in suit.

PATENTS

11. Infringement — Construction of claims (§120.03)

Patent construction — Claims — Defining terms (§125.1305)

Clause, in claims for electrically programmable read-only memory employing redundant cells and sidewall shields to inhibit erasure of cells by ultraviolet radiation, stating that such EPROM can be "permanently programmed" so that redundant elements are always used in place of any defective elements, should not be construed to require that shielded cells be at least as reliable as any other portions of EPROM, or that shielded cells withstand 300 hours of ultraviolet light exposure, since claims contain no such limitations; clause is properly construed to require only that shielded cells not be erased during normal life span of EPROM.

12. Patentability/Validity — In general (§115.01)

U.S. International Trade Commission — Procedure (§155.02)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Defenses — Estoppel (§410.1805)

International Trade Commission properly concluded that assignor estoppel should be considered and applied in cases brought under 19 USC 1337 to exclude articles which infringe U.S. patents, since 19 USC 1337(c) states that all legal and equitable defenses may be presented in Section 1337 cases, and since commission's public interest responsibilities do not give it independent duty to determine patent validity if no party has made such challenge.

PATENTS

13. Patentability/Validity — In general (§115.01)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Defenses — Estoppel (§410.1805)

Respondent in exclusion action brought under 19 USC 1337 is precluded by doctrine of assignor estoppel from challenging valid-

specification and prosecution history in suit.

ENTS

Infringement — Construction of claims (§120.03)

ent construction — Claims — Defining terms (§125.1305)

use, in claims for electrically programmable read-only memory employing redundant cells and sidewall shields to inhibit gate cells by ultraviolet radiation, stating such EPROM can be "permanently damaged" so that redundant elements always used in place of any defective cells, should not be construed to require shielded cells be at least as reliable as other portions of EPROM, or that cells withstand 300 hours of ultraviolet exposure, since claims contain no limitations; clause is properly construed to require only that shielded cells not be during normal life span of EPROM.

Entitability/Validity — In general (§115.01)

International Trade Commission — Procedure (§155.02)

CIAL PRACTICE AND DURE

cedure — Defenses — Estoppel (§10.1805)

International Trade Commission properly held that assignor estoppel should be red and applied in cases brought under USC 1337 to exclude articles which U.S. patents, since 19 USC 1337(c) that all legal and equitable defenses presented in Section 1337 cases, and commission's public interest responsibility do not give it independent duty to the patent validity if no party has such challenge.

NTS

Entitability/Validity — In general (§15.01)

CIAL PRACTICE AND DURE

ture — Defenses — Estoppel (§10.1805)

endent in exclusion action brought under USC 1337 is precluded by doctrine of estoppel from challenging valid-

ity of complainant's patent, since inventor who assigned patent to complainant was president, chief executive officer, and single largest shareholder in co-respondent corporation, and since balance of equities requires finding of privity between assignor and respondent in view of co-respondent's direct transfer of technology to respondent, inventor/assignor's continuous involvement in joint development program by two respondents which resulted in creation of accused products, assignor's indemnification of respondent, and respondent's financial involvement in co-respondent and joint development program.

14. Procedure — Judicial review — Standard of review — Patents (§410.4607.09)

Determination of literal infringement is question of fact, as is determination of equivalent structure under 35 USC 112, paragraph 6.

PATENTS

15. Infringement — Literal infringement (§120.05)

Patent construction — Claims — Means (§125.1307)

"First biasing means" in accused electrically programmable read-only memory performs same function as that in claim for sensing amplifier in floating gate memory device, even though biasing means of accused device does not have indicated "low" potential specified in claim, since first biasing means limitation of claim is not for purpose of assisting column line to which it is wired to reach low potential, but rather to limit decrease in voltage, and since biasing means on circuit in accused device similarly limits voltage decrease.

16. Infringement — Literal infringement (§120.05)

Infringement — Doctrine of equivalents — In general (§120.0701)

Patent construction — Claims — Means (§125.1307)

Consideration of prior art is not required in applying "means plus function" paragraph of 35 USC 112, since sole question is whether single means in accused device which performs function stated in claim is same as or equivalent to corresponding structure described in specification, and since prior art thus will not limit scope of claim even if it discloses equivalent structure; consideration of prior art is proper in determin-

ing infringement under doctrine of equivalents, since in that situation prior art restricts extent to which patent can be equitably extended beyond claims to cover accused device, but policies underlying such analysis are not served by restricting claim limitations in same manner under paragraph six of 35 USC 112.

17. Infringement — Literal infringement (§120.05)

Patent construction — Claims — Means (§125.1307)

International Trade Commission's holding that means of controlling voltage level on column line in accused electrically programmable read-only memory is structurally equivalent to that described in patent is affirmed, since commission found extensive similarities between relevant circuits in patented and accused devices and heard expert testimony from both sides concerning alleged distinctions between circuits, since means used by accused and claimed devices need only be equivalent, not identical, and since it cannot be held that commission's findings were unsupported by substantial evidence.

18. U.S. International Trade Commission — Appeals (§155.09)

International Trade Commission's decision on validity and infringement of earlier-issued patent, in limited exclusion order directed solely at parties before it, need not be reviewed on appeal if order is found to be fully supported by other, more recently issued patents, and commission's decision which has been appealed but which is not necessary to support scope and duration of exclusion order will consequently be vacated.

Particular patents — Electrical — Read-only memories

4,685,084, Canepa, apparatus for selecting alternate addressing mode and read-only memory, determination holding patent infringed and not invalid affirmed.

4,519,050, Folmsbee, radiation shield for an integrated circuit memory with redundant elements, determination holding patent infringed and not invalid affirmed.

4,223,394, Pathak and Perlegos, sensing amplifier for floating gate memory devices, determination holding claim 2 infringed and not invalid affirmed; determination holding claim 1 invalid vacated.

4,103,189, Perlegos and Salsbury, metal-oxide-semiconductor (MOS) buffer circuit, determination holding patent infringed and not invalid vacated.

3,938,108, Salsbury and Perlegos, erasable programmable read-only memory, determination of non-infringement vacated.

Particular patents — General and mechanical — Memory devices

4,114,255, Salsbury, Perlegos, and Morgan, floating gate storage device and method of fabrication, determination of non-infringement vacated.

Appeal from opinion and order of the U.S. International Trade Commission.

Investigation by U.S. International Trade Commission in response to complaint filed by Intel Corp. alleging unfair acts and unfair methods of competition under Tariff Act's Section 337, 19 USC 1337, by General Instrument Corp. and Microchip Technology Inc., and Atmel Corp. From entry of limited exclusion order, parties cross-appeal, with SEEQ Technologies Inc. and Hyundai Electronics Industries Co. intervening as appellees. Affirmed in part, reversed in part, and vacated in part.

Related decision: 13 USPQ2d 1547.

James J. Elacqua, of Arnold, White & Durkee, Houston, Texas (Jack C. Goldstein, Hilary E. Pearson, Timothy N. Trop, Thomas A. Miller, Danny L. Williams, Russell T. Wong, Anne E. Brookes, and Richard L. Stanley, Houston, with him on brief; Carl Silverman, Santa Clara, Calif., of counsel), for Intel Corp.

Judith M. Czako (Lyn M. Schlitt, general counsel, James A. Toupin, assistant general counsel, and John M. England, Jr., with her on brief), for U.S. International Trade Commission.

Robert C. Morgan, of Fish & Neave (Thomas L. Secrest, Wayne M. Kennard, and Gerry Ann Fifer, with him on brief), New York, N.Y., for Atmel Corp.

Stephen B. Judlowe, of Hopgood, Calma, Kalil, Blaustein & Judlowe (Marvin N. Gordon, Brian P. Murphy, and Joel Miller, with him on brief), New York, for General Instrument Corp. and Microchip Technology Inc.

James W. Geriak and Thomas J. Morgan, of Lyon & Lyon, Los Angeles, Calif., for SEEQ Technology Inc.

Philip J. Mause, of Thelen, Marrin, Johnson & Bridges, Washington, D.C., for Hyundai Electronics Industries.

Before Cowen, senior circuit judge, and Archer and Mayer, circuit judges.

Archer, J.

Intel Corporation (Intel), Atmel Corporation (Atmel), and General Instrument Corporation and Microchip Technology Incorporated (collectively GI/M) have each filed an appeal from certain aspects¹ of the Opinion (Decision) and Order, issued March 16, 1989, by the United States International Trade Commission (Commission), in *Certain Erasable Programmable Read Only Memories, Components Thereof, Products Containing Such Memories, And Processes For Making Such Memories*, Inv. No. 337-TA-276, USITC Pub. No. 2196 (Mar. 16, 1989). The Order prohibited Atmel and GI/M (and other parties in that proceeding) from importing into the United States certain Erasable Programmable Read-Only Memories (hereinafter EPROMs)² found to infringe one or more of Intel's United States patents.³ We affirm-in-part, reverse-in-part, and vacate-in-part.

I

An investigation was begun by the Commission in September 1987, under section 337 of the Tariff Act of 1930, codified as amended at 19 U.S.C. § 1337 (1988), in response to a complaint filed by Intel alleging unfair acts and unfair methods of competition in the importation and sale of certain EPROMs by seven respondents, including Atmel and GI/M. See 19 U.S.C. § 1337(a)(1) (1988).

In the complaint, Intel alleged that the respondents violated section 337 by importing EPROMs which infringed six Intel U.S.

¹ Hyundai Electronics Industries Co., Ltd. also appealed from the ITC's decision on issues unrelated to this appeal. See *Hyundai Elecs. Indus. Co. v. United States Int'l Trade Comm'n*, 899 F.2d 1204, 14 USPQ2d 1396 (Fed. Cir. 1990).

² As stated by the Commission:

[An EPROM] is a monolithic integrated circuit containing thousands of metal oxide semiconductor (MOS) transistor cells on which encoded binary information can be stored. Decision at 12 (footnote omitted).

³ The patents at issue (the Intel patents) are U.S. Patent Nos. 3,938,108 (the '108 patent); 4,048,518 (the '518 patent); 4,103,189 (the '189 patent); 4,114,255 (the '255 patent); 4,223,394 (the '394 patent); 4,519,050 (the '050 patent); and 4,685,084 (the '084 patent).

wen, senior circuit judge, and Arthur Mayer, circuit judges.

J.

orporation (Intel), Atmel Corporation, and General Instrument Corporation and Microchip Technology Incorporated (collectively GI/M) have each filed a complaint challenging certain aspects¹ of the Commission's Decision and Order, issued March 1988 by the United States International Trade Commission (Commission), in *Certifiable Programmable Read Only Memory Components Thereof, Products Using Such Memories, And Processes for Making Such Memories*, Inv. No. 76, USITC Pub. No. 2196 (March 1988). The Order prohibited Atmel and other parties in that proceeding from importing into the United States certifiable Programmable Read-Only Memories (hereinafter EPROMs)² found to be one or more of Intel's United States patents.³ We affirm-in-part, reverse-in-part, and vacate-in-part.

I

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EPROM] is a monolithic integrated circuit containing thousands of metal oxide semiconductor (MOS) transistor cells on which binary information can be stored.

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patents at issue (the Intel patents) are:

1. Nos. 3,938,108 (the '108 patent); 2. (the '394 patent); 4,103,189 (the '189 patent); 4,114,255 (the '255 patent); 4,223,394 (the '518 patent); 4,519,050 (the '050 patent); 5,084 (the '084 patent).

product patents and two Intel U.S. process patents (one of which was withdrawn from consideration).⁴ Section 337 permits the Commission to exclude from the United States any goods that violate the provisions of that section. 19 U.S.C. § 1337(e)(1). The Commission may also order any party violating section 337 "to cease and desist from engaging in the unfair methods or acts involved." 19 U.S.C. § 1337(f)(1).

The respondents challenged the validity and enforceability of the asserted patents, as well as Intel's allegations of infringement. The investigation was assigned to an admin-

istrative law judge (ALJ) who produced a 350-page initial determination (ID) detailing the facts and resolving the numerous issues presented by the parties. On review of the ID, the Commission affirmed many of the ALJ's determinations, ordered review of certain portions of the ID, and requested written submissions on those and other issues. In another prodigious effort, the Commission made 143 pages of additional findings and conclusions. The following table summarizes how the Commission disposed of the validity and infringement issues for each of the Intel patents:⁵

Patent No.	Proved Invalid?	Proved Infringed?			
		64K	256K	51 Series ⁶	1024K
'084	No	N/A	N/A	Old - Yes New - No	N/A
'050	No	Yes	Yes	Yes	No
'394	Claim 1 - Yes Claim 2 - No	Yes	No	Yes	Yes
'255	No	No	No	No	No
'189	No	N/A	Yes	N/A	N/A
'518	No	No	No	No	No
'108	No	No	No	No	No

On the basis of its Decision, the Commission entered a limited exclusion order preventing the importation of, *inter alia*, the EPROMs manufactured abroad by or for Atmel (64K, 256K, 51 Series, and 1024K), and GI/M (256K and 51 Series). Order at 7-8. In addition, the Commission ordered Atmel and GI/M to cease and desist from "importing, selling for importation, assembling, testing, performing manufacturing steps with respect to, using, marketing, distributing, offering for sale, or selling" EPROMs which were determined to be infringing. Decision at 5.

The issues before us on appeal and cross-appeal include: (1) Atmel's claim that its EPROMs are noninfringing because they are manufactured by Sanyo Electric Co.,

Ltd. and Tokyo Sanyo Electric Co., Ltd. (collectively Sanyo) under a broad cross-licensing agreement between Sanyo and Intel; (2) Atmel's claim that the '084 patent is invalid; (3) Atmel's and GI/M's challenge to the Commission's finding that their "old" 51 Series EPROM's infringe the '084 patent; (4) Atmel's and GI/M's claim that Intel's '050 patent is invalid and not infringed; (5) GI/M's challenge to the validity of claim 2 of the '394 patent; (6) Intel's argument that GI/M cannot challenge the '394 patent's validity because of the doctrine of assignor estoppel; and (7) Atmel's and GI/M's claim

¹ Although the Commission's Decision also covered other issues in addition to validity and infringement, they have not been appealed.

² The term "51 Series" appears throughout this opinion to denote Atmel and GI/M 512K, 513K and/or 515K EPROMs, which the parties and the Commission treated as alike.

³ Following Intel's complaint, Atmel and GI/M changed the design of their 51 Series EPROMs in order to avoid infringing the '084 patent. The Commission found that the former 51 Series EPROMs infringed claim 1 under the doctrine of equivalents, but that the modified version did not. Intel does not challenge the finding of noninfringement.

⁴ Atmel and GI/M manufacture and import EPROMs which have been characterized primarily by their respective memory capacities. Generally speaking, the imported EPROMs are either 256K chips (the 256K EPROMs) or 512K, 513K, and 515K chips (the 51 Series EPROMs). Chips having other memory capacities (64K and 1024K) have been alleged to infringe some of the asserted patents. Only Atmel imports the 64K and the 1024K EPROMs.

that their EPROMs do not infringe claim 2 of the '394 patent.¹

II

A. Atmel argues that its EPROMs did not infringe any of the Intel patents because the EPROMs were made by Sanyo under Sanyo's cross-licensing agreement with Intel (the Intel/Sanyo agreement). The agreement grants Sanyo the right to make, use and sell "any Sanyo . . . products" under Intel's patents. Intel contends that Sanyo is not licensed to manufacture another corporation's goods, i.e., under industry terminology Sanyo may not act as a "foundry." Because Intel licensed only *Sanyo* products,² Intel argues that the cross-license did not authorize Sanyo to manufacture Atmel-designed EPROMs for Atmel, for that would be the manufacture of "Atmel" products rather than "Sanyo" products. The ALJ framed the license defense issue as "whether Sanyo was licensed by Intel to make an Atmel EPROM, using Atmel's design, putting Atmel's name and product designation on the EPROM,

and selling the EPROM to Atmel for resale as an Atmel product." ID at 25.

If the Intel/Sanyo agreement permits Sanyo to act as a foundry for another company for products covered by the Intel patents, the purchaser of those licensed products from Sanyo would be free to use and/or resell the products. Such further use and sale is beyond the reach of the patent statutes. See *United States v. Univis Lens Co.*, 316 U.S. 241, 250-52 [53 USPQ 404] (1942) (the first vending of any article manufactured under a patent puts the article beyond the reach of the patent).

Section 14.5 of the Intel/Sanyo agreement states that "[t]his Agreement shall be governed by and subject to and construed according to the laws of the State of California." Under California law, the interpretation of a contract is a question of law, to the extent that it is based on the language of the agreement. *Clark v. Rancho Santa Fe Ass'n*, 216 Cal. App.3d 606, 618, 265 Cal. Rptr. 41, 47 (1989); see also *Kern Oil & Refining Co. v. Tenneco Oil Co.*, 840 F.2d 730, 736 (9th Cir. 1988). When interpreting a contract, we must, where possible, give meaning and purpose to every term used in the contract. See, e.g., *Beck v. American Health Group Int'l, Inc.*, 211 Cal. App.3d 1555, 1566, 260 Cal. Rptr. 237, 244 (1989) (citing *Jensen v. Traders & General Ins. Co.*, 52 Cal. 2d 786, 345 P.2d 1 (1959)); see also *Fortec Constructors v. United States*, 760 F.2d 1288, 1292 (Fed. Cir. 1985). In resolving what the parties meant by limiting the license only to Sanyo products, we try to ascertain and give effect to the intent of the parties at the time the contract was signed. See *Moss Dev. Co. v. Geary*, 41 Cal. App.3d 1, 9, 115 Cal. Rptr. 736, 741 (1974); Cal. Civ. Code §§ 1636, 1641, 1652-53 (1985); see also *Ralden Partnership v. United States*, 891 F.2d 1575, 1577 (Fed. Cir. 1989).

In determining that the Intel/Sanyo agreement did not cover foundry rights, the ALJ reasoned:

It is reasonable to assume that the parties meant to exclude parts that one party made as foundry for another company, using the other company's design, parts intended to be sold as the other company's parts under the other company's name, and not just used as Sanyo components in a larger product made by another company.

The interpretation of the licensing agreement as proposed by Atmel would mean that any company that was unable to obtain a license from Intel but still wanted to make its own parts practicing

¹We do not reach GI/M's challenge to the Commission's finding that the '189 patent was valid and infringed. Nor do we reach Intel's challenge to the Commission's findings that Intel's '255 patent was not infringed, and that claim 1 of its '394 patent was proven invalid. See discussion, *infra* pp. 52-53; see also *Texas Instruments Inc. v. United States Int'l Trade Comm'n*, 871 F.2d 1054, 1067, 10 USPQ2d 1257, 1267 (Fed. Cir. 1989).

²The cross-licensing agreement between Intel and Sanyo contains the following clauses related to Atmel's defense:

3.5 Intel hereby grants and will grant to Sanyo an [sic] non-exclusive, world-wide royalty-free license without the right to sublicense except to its Subsidiaries, under Intel Patents which read on any Sanyo Semiconductor Material, Semiconductor Device, Magnetic Bubble Memory Device, Integrated Circuit and Electronic Circuit products, for the lives of such patents, to make, use and sell such products.

3.6 Sanyo hereby grants and will grant to Intel a non-exclusive, world-wide, royalty-free, license without the right to sublicense except to its Subsidiaries, under Sanyo Patents which read on any Intel Semiconductor Material, Semiconductor Device, Magnetic Bubble Memory Device, Integrated Circuit and Electronic Circuit products, for the lives of such patents to make, use and sell such products.

3.8 Except as expressly provided herein there are no other licenses, by implication, estoppel or otherwise granted by Intel to Sanyo. (Emphases added.) [No. 89-1476, Exhibits E13360-61]

selling the EPROM to Atmel for resale at Atmel product." ID at 25. The Intel/Sanyo agreement permits Atmel to act as a foundry for another company for products covered by the Intel patents, the purchaser of those licensed products Sanyo would be free to use and/or sell the products. Such further use and sale beyond the reach of the patent statutes. *United States v. Univis Lens Co.*, 316 F.2d 241, 250-52 [53 USPQ 404] (1942) (first vending of any article manufactured under a patent puts the article beyond the reach of the patent).

Section 14.5 of the Intel/Sanyo agreement states that "[t]his Agreement shall be governed by and subject to and construed according to the laws of the State of California. Under California law, the interpretation of a contract is a question of law, to the extent that it is based on the language of the agreement. *Clark v. Rancho Santa Fe Ass'n*, Cal. App.3d 606, 618, 265 Cal. Rptr. 41, 1989); see also *Kern Oil & Refining Co. v. Pennoco Oil Co.*, 840 F.2d 730, 736 (9th Cir. 1988). When interpreting a contract, we, where possible, give meaning and purpose to every term used in the contract. See, *Beck v. American Health Group Int'l*, 211 Cal. App.3d 1555, 1566, 260 Cal. 2d 237, 244 (1989) (citing *Jensen v. Insurers & General Ins. Co.*, 52 Cal. 2d 786, P.2d 1 (1959)); see also *Fortec Contractors v. United States*, 760 F.2d 1288, 1302 (Fed. Cir. 1985). In resolving what is meant by limiting the license only to certain products, we try to ascertain and give effect to the intent of the parties at the time the contract was signed. See *Moss Dev. Co.*, 41 Cal. App.3d 1, 9, 115 Cal. Rptr. 741 (1974); Cal. Civ. Code §§ 1636, 1652-53 (1985); see also *Ralden Partnership v. United States*, 891 F.2d 1575, (Fed. Cir. 1989).

determining that the Intel/Sanyo agreement did not cover foundry rights, the parties reasonably assumed that the parties

wanted to exclude parts that one party made as foundry for another company, using the other company's design, parts intended to be sold as the other company's parts under the other company's name, and not just used as Sanyo components in larger products made by another company.

The interpretation of the licensing agreement as proposed by Atmel would mean that any company that was unable to obtain a license from Intel but still wanted to make its own parts practicing

Intel patents could employ Sanyo as a foundry and circumvent Intel's patents. *Without something to explain why the parties would have intended such a result, the agreement will not be given this strained construction.*

ID at 28 (citation omitted, emphasis added). By not reviewing the ALJ's decision on this issue, the Commission adopted that decision. Commission Rule 210.53(h), 53 Fed. Reg. 33,070 (1988) (codified at 19 C.F.R. § 210.53(h) (1990)).

While there is no indication in the agreement as to what the parties meant by the "Sanyo" limitation, the use of that language in paragraph 3.5 clearly evinces that the parties intended to restrict the grant in some manner.

Atmel argues that the "Sanyo" limitation in paragraph 3.5 was only intended to prevent the transfer of "have made" rights to Sanyo, i.e., to prevent Sanyo from hiring another company to manufacture licensed products for Sanyo. Atmel urges that its interpretation of paragraph 3.5 is supported by a letter containing a summary of the amendments prepared by a member of Intel's negotiating team in connection with a later extension of the Intel/Sanyo agreement. This letter describes the amended agreement as being unchanged insofar as it is a "[g]eneral patent cross license without 'have made' rights."¹⁰ In this connection, Atmel contends that paragraph 3.8 cannot be read as excluding "have made" rights. Further, it argues that if any portion of the contract excludes "have made" rights, as suggested in the letter, it must be the "Sanyo" limitation in paragraph 3.5. Finally, because the letter expressly states that the agreement excludes "have made" rights and fails to say that foundry rights are similarly excluded, Atmel draws the conclusion that Intel believed its license to Sanyo included foundry rights.

Although the ALJ did not specifically mention the letter,¹¹ she did fully consider and reject Atmel's arguments regarding the source of the "have made" exclusion. In

referring to paragraph 3.8, the ALJ said that neither party intended to rely upon any implied license from Intel to Sanyo and that this provision "prevent[s] any implication of 'have made' rights under the license." ID at 24. Noting that there was no evidence indicating that Intel knew Sanyo might act as a foundry for other unlicensed companies, that Sanyo's license in paragraph 3.5 was worldwide and royalty-free, and that Intel would not receive any further consideration no matter how many companies went to Sanyo for parts that infringed Intel patents, the ALJ posed the hypothetical question: Could Intel have intended that any company in the world could get Sanyo to make its parts without having to get its own license from Intel on Intel's patents? The ALJ's answer was that, in the absence of evidence of any such intent on the part of the parties to the contract, this construction of the license agreement would not be adopted. The ALJ concluded:

The language at issue in the license agreement lends itself to another meaning that is more plausible: that both parties intended that Sanyo and Intel would have the right to make, use and sell their own parts without the constraints imposed by the patent rights of the other party.

It seems unlikely that the word "Sanyo" was used here to prevent Sanyo from having parts that use Intel patents made for Sanyo by others. The license already prevents the implication of "have made" rights. The use of the word "Sanyo" to impose a restriction against "have made" rights would have been ambiguous and not the customary way to express this restriction.

ID at 27.

[1] We agree that Atmel has not established its license defense to infringement, and that the ALJ's reasoning is persuasive. Moreover, the ALJ's interpretation is consistent with other provisions of the agreement.

The language of paragraph 3.5 grants Sanyo a world-wide, royalty-free license to practice "Intel Patents." The agreement defines the term "Intel Patents" broadly, covering "any and all" patents that Intel "owns or controls," including those of its subsidiaries. The only limitations in paragraph 3.5 are that Sanyo (1) may not sublicense, except to subsidiaries, and (2) may only make, use and sell "Sanyo . . . products." Atmel's argument is that the "Sanyo" limitation precludes only "have made" rights, and Sanyo otherwise has an unlimited, royalty-free right to practice all Intel patents. Put another way, any

¹⁰ The amended Intel/Sanyo agreement did not change the cross-licensing paragraphs 3.5, 3.6, or 3.8 at issue. Moreover, as in the case of the original Intel/Sanyo agreement, there is no explicit mention of foundry rights.

¹¹ The ALJ may not have mentioned the letter because of its lack of probative value. We have not been given any record references indicating the circumstances under which the letter was prepared, the position and authority of the author and addressees, or the actual distribution of the letter.

thing manufactured by Sanyo that utilizes any Intel patent is subject to the royalty-free license of paragraph 3.5.

Atmel's interpretation, however, tends to create an internal inconsistency in the agreement. Paragraph 4.3 and 4.4 of the agreement require that Sanyo pay royalties to Intel on the sales of specific Intel chips made by Sanyo and on derivative products based on those chips, whether developed jointly or by Sanyo. Interpreting paragraph 3.5 as broadly as Atmel desires would encompass these chips and derivative products as royalty-free. For consistency of the agreement as a whole, the words "Sanyo . . . products" as used in paragraph 3.5 are properly construed to cover only Sanyo designed and manufactured products and to exclude parts designed by others.

Such a consistent reading precludes the royalty-free, foundry manufacture by Sanyo of an "Atmel EPROM, using Atmel's design, putting Atmel's name and product designation on the EPROM, and selling the EPROM to Atmel for resale as an Atmel product." ID at 25. Atmel had the burden of proving its defense to infringement, *Met-Coil Sys. Corp. v. Korners Unlimited, Inc.*, 803 F.2d 684, 687, 231 USPQ 474, 476 (Fed. Cir. 1986), and we are convinced that the Commission properly determined that Atmel failed to do so.

III

Turning now to the Commission's holdings as to validity and infringement issues, we will consider the Intel patents in the reverse order of issuance.¹²

¹² The Commission argues that GI/M's petition to the Commission for review of the ID was defective in that it failed to identify which of the ALJ's findings of fact or conclusions of law were being challenged, as required by Commission rule. See 19 C.F.R. § 210.54(a)(ii). As a result, the Commission contends that GI/M abandoned these issues below and is not entitled to have this court review them.

We disagree. Clearly GI/M petitioned the Commission for a review of the ALJ's findings on GI/M's alleged infringement of Intel's '084 patent. GI/M's petition also stated "[w]ith respect to five other patents, the '108, '518, '394, '084, '189 and '255 patents, the . . . respondents refer the Commission to their Post Trial, Main, and Reply Briefs on those patents and incorporate those briefs herein by reference." While the incorporation of previously submitted briefs in a petition for review may not be optimal, it would be unfair to say that GI/M has "knowingly abandoned or waived" the issues related to these patents, see *James v. Federal Energy Regulatory Comm'n*, 755 F.2d 154, 155 (Fed. Cir. 1985), particularly since the Commission accepted

A. The '084 Patent

The '084 patent issued on August 4, 1987, and relates to "circuitry for enabling an EPROM to be programmed selectively for addressing either the full memory array (i.e., in a 'non-page mode') or for addressing the array by 'pages' (i.e., in a 'page mode')."
Decision at 79.

1. Validity of the '084 patent

Atmel¹³ argues that the '084 patent is invalid because the 27C512/13 EPROMs which embody the invention were placed on sale more than a year before the application's filing date of June 7, 1985. 35 U.S.C. § 102(b) (1988). Under 35 U.S.C. § 282 a patent is presumed valid, and proof of its invalidity requires "clear and convincing" evidence. *Buildex, Inc. v. Kason Indus., Inc.*, 849 F.2d 1461, 1463, 7 USPQ2d 1325, 1326-27 (Fed. Cir. 1988).

It is undisputed that Intel distributed the 27C512/13 EPROMs to its sales force prior to June 7, 1984, the critical, or statutory bar, date, and that the chips were eventually sold to Intel's customers. The sole issue is whether any sales or offers to sell took place before the critical date. See *In re Caveney*, 761 F.2d 671, 676, 226 USPQ 1, 4 (Fed. Cir. 1985). The ALJ made the following findings:

[A] sales conference was held in Phoenix, Arizona during the week of May 15, 1984. At that meeting 50 samples of the Intel 27C512/13 were distributed to 50 Intel salesmen.

The Intel sales conference in Phoenix was attended only by Intel personnel. . . . At the Phoenix conference, no sales person was allowed to take more than one 27C512/13 [sic] sample.

Each of the samples given to the Intel salesmen at the Phoenix meeting during the week of May 15, 1984, about three weeks before the statutory bar, included the page mode circuit described and claimed in the '084 patent. No restriction was placed on the Intel salesmen as to how they could dispose of the 27C512/13 samples. The salesmen were expected to pass the samples on to their customers.

GI/M's petition for review and considered and decided the issues therein. Decision at 2. GI/M is entitled to judicial review of the Commission's conclusions.

¹³ GI/M does not challenge the validity of the '084 patent, although it does argue that its chips did not infringe that patent.

1. The '084 Patent

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Decision at 79.

2. Validity of the '084 patent

Atmel¹¹ argues that the '084 patent is valid because the 27C512/13 EPROMs which embody the invention were placed on the market more than a year before the application's filing date of June 7, 1985. 35 U.S.C. § 102(b) (1988). Under 35 U.S.C. § 282 a patent is presumed valid, and proof of its invalidity requires "clear and convincing" evidence. *Buildex, Inc. v. Kason Indus., Inc.*, 816 F.2d 1461, 1463, 7 USPQ2d 1325, 6-27 (Fed. Cir. 1988).

It is undisputed that Intel distributed the 27C512/13 EPROMs to its sales force prior to June 7, 1984, the critical, or statutory bar, and that the chips were eventually sold to Intel's customers. The sole issue is whether any sales or offers to sell took place before the critical date. See *In re Caveney*, 761 F.2d 676, 226 USPQ 1, 4 (Fed. Cir. 1985). The ALJ made the following findings:

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¹¹ Petition for review and considered and decided the issues therein. Decision at 2. G1/M is not to judicial review of the Commission's actions.

G1/M does not challenge the validity of the patent, although it does argue that its chips infringe that patent.

Intel was seeking commercial advantage by its distribution of 27512 [sic] samples before the critical date. Intel was trying to catch up with AMD [a competitor] in the marketplace.

... Intel's engineering samples are pre-production samples that are not available for sale. The Intel sales activities at and after the Phoenix meeting were clearly commercial in intent, however, and if it were clear that they occurred before the critical date, they would constitute an on-sale bar under 35 U.S.C. § 102(b). The distribution of the 512/13 samples to Intel customers before the critical date would constitute an on-sale bar against the validity of the patent pursuant to 35 U.S.C. § 102(b), but respondents did not prove by clear and convincing objective evidence that any of these customers in fact received the part before June 7.

Decision at 236-40 (citations omitted, emphasis added).

The Commission, in agreeing that Atmel had failed to establish the on-sale bar defense, stated:

[W]e agree] with the ALJ that respondents failed to prove the existence of an invalidating on-sale bar under 35 U.S.C. § 102(b). One would have to engage in extensive inference drawing to conclude that Intel's 27C512/513 part was actually sold or offered for sale more than a year prior to the filing of the application that matured into the '084 patent. Such inference drawing does not in the Commission's view rise to the level of clear and convincing evidence. The Commission adopts the ALJ's factual findings and conclusions of law to the extent they are not inconsistent with the Commission's determination.

Decision at 84 (emphasis added).

[2] Whether a particular activity raises the on-sale bar is a question of law, based on underlying factual considerations. See, e.g., *J.A. LaPorte, Inc. v. Norfolk Dredging Co.*, 787 F.2d 1577, 229 USPQ 435 (Fed. Cir. 1986); *Shatterproof Glass Corp. v. Libbey-Owens Ford Co.*, 758 F.2d 613, 225 USPQ 634 (Fed. Cir. 1985).

The "on-sale" bar encourages early disclosure and prevents extension of the statutory patent term. See *King Instrument Corp. v. Otari Corp.*, 767 F.2d 853, 226 USPQ 402 (Fed. Cir. 1985). A single sale or offer to sell is enough to bar patentability. *Caveney*, 761 F.2d at 676, 226 USPQ at 4. Even free distribution of a prototype may raise the on-sale bar if it is done to solicit a sale. *Stearns v. Beckman Instruments, Inc.*, 737 F.2d 1565, 222 USPQ 457 (Fed. Cir. 1984).

[3] Atmel argues that the ALJ made all the findings necessary to raise the on-sale bar — (1) that the claimed invention was reduced to practice by Intel prior to the critical date; (2) that three weeks before the critical date, Intel gave the EPROMs embodying the claimed invention to salesmen; (3) that these salesmen were expected to distribute the samples to their customers; and (4) that Intel was seeking a commercial advantage by its distribution of samples before the critical date.

Although these findings may go far toward establishing an on-sale bar, they are insufficient, standing alone, for us to conclude that the Commission erred in refusing to find that any 512/13-type EPROMs were actually sold or offered for sale to Intel's customers. The ALJ found that, while it was "likely" that Intel's customers received the EPROMs before the critical date, Atmel had not proven this by clear and convincing evidence. Intel's distribution of the EPROMs to its own sales staff did not constitute a statutory bar. It is not a violation of the on-sale bar to make preparations for the sale of a claimed invention — an actual sale or offer to sell must be proved. 35 U.S.C. § 102(b). See also *UMC Elec. Co. v. United States*, 816 F.2d 647, 2 USPQ2d 1465 (Fed. Cir. 1987).

Atmel offered no evidence, direct or circumstantial, showing that Intel made offers or sales before the initial date. All Atmel proved was that such offers or sales may have been "likely." As the Commission pointed out, "[o]ne would have to engage in extensive inference drawing to conclude that Intel's 27C512/513 part was actually sold or offered for sale more than a year prior to the filing of the application." Decision at 84. Clear and convincing evidence has been described as evidence which proves in the mind of the trier of fact "an abiding conviction that the truth of [the] factual contentions are [sic] 'highly probable.'" *Colorado v. New Mexico*, 467 U.S. 310, 316 (1984) (citation omitted); see also *Buildex*, 849 F.2d at 1463, 7 USPQ2d at 1326-27. The extensive inferences Atmel would draw from the evidence presented are not the clear and convincing proof required. Thus, Atmel has failed to carry its burden of proof that a sale or offer to sell was made before June 7, 1984. 35 U.S.C. § 282; see also *UMC*, 816 F.2d at 657, 2 USPQ2d at 1472. Accordingly, we affirm the Commission's determination that the '084 patent was not proven to be invalid.

2. Infringement of the '084 patent

Before the Commission, Intel alleged that Atmel's and GI/M's "old" design 51 Series EPROMs infringed claims 1-10 of the '084 patent and that their "new" design 51 series EPROMs infringe claims 1-4. Intel did not assert that any other EPROMs infringe the '084 patent. The ALJ determined that both Atmel's and GI/M's "old" design 51 Series EPROMs infringed claim 1 of the '084 patent under the doctrine of equivalents, but that the "new" design 51 Series EPROMs did not infringe that patent. On review, the Commission affirmed both decisions.¹⁴

The '084 patent discloses an integrated circuit read-only memory with a programmable selection means for selecting alternative addressing modes. Claim 1 of the '084 patent reads:

1. In an integrated circuit, read-only memory having n address lines used for accessing p words in one addressing mode, an improvement for providing an alternate addressing mode, comprising:

programmable selection means for selecting said alternate addressing mode; storage means for storing at least one signal;

an address buffer coupled to one of said n address lines, said buffer also being coupled to said storage means and said programmable selection means, the output of said buffer being controlled by said signal stored in said storage means when said alternate addressing mode is selected, whereby when said alternate addressing mode is selected said p words in said memory may be selected with less than n address signals.

In construing this claim, the ALJ stated: The special circuit disclosed in the '084 patent permits the address buffer to accept either input from the storage means or from the address line. (Huber Tr. 4783.) Which one is selected depends on whether page mode addressing has been selected. In non-page mode, the address buffer accepts the signal from the address

line. In page mode, the address buffer accepts the signal stored in the latch. (Intel Ex. 15, col. 3, lines 5-18; Huber Tr. 4783.)

The special address buffer disclosed in the patent can perform normal address input signal processing, it can receive the logic signal stored in the latch, it can send a signal derived either from the address input or from the latch input, and it can implement page mode addressing when directed to do so by the programmable selection means. (Huber Tr. 4782-84.)

ID at 249-50. The ALJ also observed:

Respondents' old '512 parts do not have an *address buffer* coupled to the storage means or latch, as that term has been construed in the patent claims. Instead . . . Atmel [] has a multiplexer. The multiplexer does not buffer the signal. It receives multiple signals and selects signals to be passed on to the decoder circuitry depending on whether the part is programmed for page mode or normal addressing. (Gust Perlegos Tr. 5064-65; Atmel Ex. 220.)

ID at 257 (emphasis in original).

Atmel's and GI/M's primary argument is that the accused device has no component which corresponds to the claimed "address buffer." The ALJ's findings make this argument unpersuasive. While it is true that the accused EPROMs use a multiplexer rather than an address buffer, the ALJ determined that the address buffer of the '084 patent contains additional circuitry to permit it to accept input from alternative sources and that this same function was performed in the accused device by a multiplexer. The ALJ expressly found that the "multiplexer . . . is the functional equivalent of the special address buffer as it is described in the '084 patent specification." ID at 259. Moreover, the ALJ found that the buffering function performed by the special address buffer of the '084 patent was performed in the accused EPROMs "in another circuit" before being stored in the latch. ID at 259. The ALJ's findings were stated as follows:

The respondents' 27C512/513/515 parts using the old designs contain each element required by claim 1 of the '084 patent except the special address buffer. They do not literally infringe claims 1-10 of the '084 patent. The fact that a buffer

¹⁴ GI/M suggests that the issue of whether its "old" design 51 Series EPROMs infringed the '084 patent was mooted by its unilateral decision to stop manufacturing the "old" design EPROMs. We disagree. The Supreme Court has stated that the "[m]ere voluntary cessation of allegedly illegal conduct does not moot a case; if it did, the courts would be compelled to leave '[t]he defendant . . . free to return to his old ways.'" *United States v. Concentrated Phosphate Export Ass'n, Inc.*, 393 U.S. 199, 203 (1968) (quoting *United States v. W.T. Grant Co.*, 345 U.S. 629, 632 (1953)).

" GI/M agreed before the Commission that Atmel's "old" design 512K EPROM was representative of their accused devices. Accordingly, the ALJ and the Commission dealt only with that device.

ie. In page mode, the address buffer accepts the signal stored in the latch. (In'l Ex. 15, col. 3, lines 5-18; Huber Tr. '83.)

The special address buffer disclosed in the patent can perform normal address signal processing, it can receive the signal stored in the latch, it can send signal derived either from the address input or from the latch input, and it can implement page mode addressing when directed to do so by the programmable selection means. (Huber Tr. 4782-84.)

At 249-50. The ALJ also observed: Respondents' old '512 parts do not have *address buffer* coupled to the storage latches or latch, as that term has been construed in the patent claims. Instead . . . Intel [] has a multiplexer. The multiplexer does not buffer the signal. It receives multiple signals and selects signals to be passed on to the decoder circuitry depending on whether the part is programmed for page mode or normal addressing. (Gust Perlegos Tr. 5064-65; At'l Ex. 220.)

257 (emphasis in original).

Intel's and GI/M's primary argument is the accused device has no component that corresponds to the claimed "address buffer." The ALJ's findings make this argument unpersuasive. While it is true that the accused EPROMs use a multiplexer rather than an address buffer, the ALJ determined the address buffer of the '084 patent has additional circuitry to permit it to accept input from alternative sources and this same function was performed in the accused device by a multiplexer. The ALJ easily found that the "multiplexer . . . is a functional equivalent of the special address buffer as it is described in the '084 patent specification." ID at 259. Moreover, the ALJ found that the buffering function performed by the special address buffer of the '084 patent was performed in the accused EPROMs "in another circuit" before being stored in the latch. ID at 259. The ALJ's findings were stated as follows:

The respondents' 27C512/513/515 are using the old designs contain each element required by claim 1 of the '084 patent except the special address buffer. They do not literally infringe claims 1-10 of the '084 patent. The fact that a buffer

GI/M agreed before the Commission that its "old" design 512K EPROM was representative of their accused devices. Accordingly, the ALJ and the Commission dealt only with that

circuit selects which signals are sent to the decoder in the embodiment in the patent does not mean that the use of a buffer circuit is a significant part of the invention and that nothing else can perform that function.

ID at 258-59. Based on these findings, the ALJ concluded that the accused EPROMs perform substantially the same function in substantially the same way to achieve substantially the same result. The Commission affirmed this conclusion, stating:

Both the multiplexer and the address buffer use an addressing signal to select a particular memory cell from an incoming address pin or latch. Thus, the accused circuits infringe claim 1 under the doctrine of equivalents because they perform substantially the same function in substantially the same way to obtain the same result as the invention claimed in the '084 patent.

Decision at 87.

[4] A finding of infringement under the doctrine of equivalents is a factual determination. *Pennwalt Corp. v. Durand-Wayland, Inc.*, 833 F.2d 931, 936, 4 USPQ2d 1737, 1741 (1987) (in banc). We review the Commission's factual findings under the substantial evidence standard. *SSIH Equip. S.A. v. United States Int'l Trade Comm'n*, 718 F.2d 365, 371-372, 218 USPQ 678, 684 (Fed. Cir. 1983). The doctrine of equivalents does not require a one-to-one correspondence between the accused device and that disclosed in the patent. In *Corning Glass Works v. Sumitomo Electric U.S.A., Inc.*, 868 F.2d 1251, 9 USPQ2d 1962 (Fed. Cir. 1989), we held that infringement under the doctrine of equivalents may be established even though the accused device requires a number of components to perform functions which the patented invention achieves by use of one component. "[T]he determination of equivalency is not subject to . . . a rigid formula. An equivalent must be found for every limitation of the claim somewhere in an accused device, but not necessarily in a corresponding component. . . ." *Id.* at 1259, 9 USPQ2d at 1968 (footnote omitted).

[5] In the hearings, the operation of both the patented invention and the allegedly infringing device were discussed at length by the witnesses. There was testimony fully supporting the ALJ's findings that the multiplexer performed the selective signal acceptance function of the claimed address buffer and that, while the multiplexer did not act as a buffer, that function was performed elsewhere in the accused EPROMs. Accordingly, we cannot say that the ALJ's and the Commission's findings that the "old" 51 Se-

ries EPROMs infringed the '084 patent under the doctrine of equivalents were not supported by substantial evidence.

[6] GI/M also contends that the Commission's finding of infringement under the doctrine of equivalents is incorrect because, although GI/M's "old" design 51 Series EPROMs are capable of performing page mode addressing, the EPROMs were never sold to operate in page mode. No customer was ever told how to convert the chip to page mode operation — or even that such conversion was possible. GI/M argues that an alleged infringer must intend its parts to be used in an infringing fashion and cites *Fromberg, Inc. v. Thornhill*, 315 F.2d 407, 415, 137 USPQ 84, 89 (5th Cir. 1963), in support of its argument. As noted by Intel, there is no intent element to *direct* infringement. See 35 U.S.C. § 271(b) and (c). *Fromberg* deals with induced and contributory infringement and is therefore inapposite. Because the language of claim 1 refers to "programmable selection means" and states "whereby when said alternate addressing mode is selected" (emphases added), the accused device, to be infringing, need only be capable of operating in the page mode. Contrary to GI/M's argument, actual page mode operation in the accused device is not required.

GI/M contends further that the Commission's finding of infringement is flawed because Intel's expert witnesses failed to opine in terms of the three-part test for the doctrine of equivalents. See *Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 607 [85 USPQ 328] (1950); *Pennwalt*, 833 F.2d at 934, 4 USPQ2d at 1739. This argument is meritless.

[7] Unlike a jury in a district court case, the Commission resolves disputes involving patent infringement matters with some regularity and thus is aware of doctrine of equivalents jurisprudence. More importantly, in this case the Commission demonstrated its awareness of the three-part test and applied it to facts here involved. The Commission expressly recited its conclusions in terms of the function, way, and results of the claimed invention and the accused devices. See Decision at 87 (quoted *ante* at p. 21). Under these circumstances, it is unimportant that the testimony before the Commission, which fully supports the Commission's analysis, was not given in the precise function-way/result terminology of *Graver Tank*.

Thus, we are not persuaded that the Commission erred in affirming the ALJ's determination that GI/M's "old" design 51 Series EPROMs infringed claim 1 of the '084 patent under the doctrine of equivalents.

B. The '050 Patent

The '050 patent, entitled "Radiation Shield For An Integrated Circuit Memory With Redundant Elements," issued on May 21, 1985. The '050 patent discloses and claims a radiation shield for converting a normally erasable EPROM cell into a *Unerasable Programmable Read-Only Memory (UPROM)* cell. ID at 191-92. A radiation shield is essentially a cover and side walls which surround the cell, protecting it from ultraviolet radiation. Claims 1-4 of the '050 patent are as follows:

1. In a metal-oxide-semiconductor (MOS) electrically programmable read only-memory (EPROM) which is fabricated on a substrate and which is erased when exposed to radiation, an improvement comprising:

redundant elements to be used in place of defective elements;

a programming means for programming said redundant elements so as to cause said redundant elements to be used in place of said defective elements, said programming means including at least one EPROM cell which is erased when exposed to radiation; and

a shielding member comprising an upper cover and upstanding members extending from said upper cover to said substrate disposed about said EPROM cell which causes radiation incident on said memory to be attenuated before striking said EPROM cell thus inhibiting said EPROM cell from being erased when said memory is exposed to radiation;

whereby said EPROM cell can be permanently programmed so that said redundant elements are always used in place of said defective elements.

2. The memory of claim 1 wherein said shielding member is disposed over the surface of said EPROM cell and extends normally into said EPROM cell at the edges of said EPROM cell so as to make contact with said substrate.

3. The memory of claim 2 wherein said shielding member is a conductor which defines an opening above the substrate so as to allow conductors connected to said EPROM cell to pass through said opening, said opening formed such that radiation entering said opening must traverse at least one angle of approximately 90 degrees before reaching source and drain regions of said cell.

4. The memory of claim 3 wherein said shielding member is connected to a diffusion region formed in said substrate, said diffusion being common with said

EPROM cell so as to reduce the number of said conductors passing through said opening.

An EPROM which was manufactured with a defective cell in the memory array generally was discarded because there was no way to keep the EPROM from trying to store information in the defective cell. The invention of the '050 patent was directed to shielding otherwise erasable cells in the EPROM from erasure so that they can be permanently programmed to direct information away from any defective memory elements and toward replacement or redundant memory cells. The memory cells in EPROMs are designed to be erased by exposure to ultraviolet radiation so they can be re-used to store new information.

In its complaint to the Commission, Intel alleged that GI/M's and Atmel's 256K and 512K EPROMs, and Atmel's 64K EPROM, contain radiation shields which infringe claims 1-4 of the '050 patent. Atmel and GI/M denied Intel's allegations and countered that the '050 patent's claims were invalid under 35 U.S.C. §§ 103 (obviousness) and 112 (indefiniteness), and were unenforceable for inequitable conduct.

The ALJ determined that the '050 patent was not proven invalid or unenforceable and was infringed by Atmel's and GI/M's accused devices. On review, the Commission modified some of the ALJ's findings and conclusions but, on the whole, affirmed "the ALJ's determination that: (1) respondents had failed to prove by clear and convincing evidence that claims 1-4 of the '050 patent are invalid, and (2) respondents' accused EPROMs . . . literally infringe claims 1-4 of the '050 patent." Decision at 74-75.

In this appeal, Atmel and GI/M claim that the invention disclosed in the '050 patent was invalid for obviousness and that the accused EPROMs do not infringe the Intel patent.

1. Validity of the '050 Patent

According to Atmel and GI/M, the first four claims of the '050 patent would have been obvious in light of the prior art and are thus invalid. As discussed earlier, a patent is presumed valid and the party asserting invalidity must overcome this presumption by clear and convincing evidence establishing facts which support the conclusion of invalidity. *See Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 810 [229 USPQ 478] (1986).

[8] Obviousness is a question of law based on a series of factual determinations, including (1) the scope and content of the prior art, (2) the differences between the art and the claims at issue, (3) the level of ordinary skill

OM cell so as to reduce the number of conductors passing through said cell. The EPROM which was manufactured defective cell in the memory array was discarded because there was to keep the EPROM from trying to information in the defective cell. The on of the '050 patent was directed to using otherwise erasable cells in the M from erasure so that they can be nently programmed to direct informa- way from any defective memory ele- and toward replacement or redundant y cells. The memory cells in Ms are designed to be erased by expo- ultraviolet radiation so they can be to store new information.

complaint to the Commission, Intel d that GI/M's and Atmel's 256K and EPROMs, and Atmel's 64K EPROM, a radiation shields which infringe 1-4 of the '050 patent. Atmel and denied Intel's allegations and coun- that the '050 patent's claims were in- under 35 U.S.C. §§ 103 (obviousness) 12 (indefiniteness), and were unen- for inequitable conduct.

ALJ determined that the '050 patent not proven invalid or unenforceable and infringed by Atmel's and GI/M's ac- devices. On review, the Commission ed some of the ALJ's findings and sions but, in the whole, affirmed "the determination that: (1) respondents bled to prove by clear and convincing ce that claims 1-4 of the '050 patent valid, and (2) respondents' accused DMs . . . literally infringe claims 1-4 of 50 patent." Decision at 74-75.

his appeal, Atmel and GI/M claim the invention disclosed in the '050 pat- is invalid for obviousness and that the ed EPROMs do not infringe the Intel

Validity of the '050 Patent

ording to Atmel and GI/M, the first claims of the '050 patent would have obvious in light of the prior art and are invalid. As discussed earlier, a patent is not valid and the party asserting in- must overcome this presumption by and convincing evidence establishing which support the conclusion of invalid- e *Dennison Mfg. Co. v. Panduit Corp.*, S. 809, 810 [229 USPQ 478] (1986). Obviousness is a question of law based eries of factual determinations, includ- the scope and content of the prior art, the differences between the art and the at issue, (3) the level of ordinary skill

in the art, and (4) any other objective evi- dence. *Graham v. John Deere Co.*, 383 U.S. 1, 17 [148 USPQ 459] (1966); see also *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1547, 220 USPQ 193, 197 (Fed. Cir. 1983). We examine the Commission's factual determinations under the substantial evi- dence standard, *SSIH*, 718 F.2d at 371-372, 218 USPQ at 684, and then review the holding of nonobviousness *de novo*. See *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987).

In the prosecution of the application that matured into the '050 patent, the claims were rejected as unpatentable over the McKenny article¹⁰ and the Du patent.¹¹ The McKenny article explained how redundant elements could be used to compensate for defective elements. The Du patent disclosed using a shielding region with erasable memory cells to protect some cells from radiation. When Intel narrowed the claims to include the extension of the shield's side walls down to the substrate, blocking horizontally-traveling radiation, the claim was allowed. The ALJ found that the side walls represent the only difference between the subject matter allowed and that previously rejected. In examining the scope of the prior art, the ALJ considered the Kondo and Katzenelson articles,¹² which taught that the use of shielding side walls would reduce the amount of light reaching the cells. The ALJ found, however, that neither of these articles taught that the side walls should extend all the way to the substrate, and that neither of these articles described a method of shielding a circuit thoroughly enough to last for the normal life of an EPROM. Cells protected in the manner described in Kondo and Katzenelson eventually erased.

Next, the ALJ found that one with ordinary skill in the art would have some experience with EPROMs and probably would have at least a Bachelor of Science degree in electrical engineering.

Finally, the ALJ examined other evidence of nonobviousness:

The prior art did not teach a shielding structure that adequately protects an

¹⁰ McKenny, "Good Bits Swapped for Bad in 64-Kilobit EPROM," *Electronics*, March, 1980.

¹¹ U.S. Patent No. 4,393,499, issued to Du et al.

¹² Kondo et al., *An Erase Model in Double Poly-Si Gate N-Channel FAMOS Devices*, IEEE Transactions on Electron Devices, March 1978, at 369-74; and Katzenelson et al., *An Erase Model for FAMOS EPROM Devices*, IEEE Transactions on Electron Devices, Sept. 1980, at 1744-52.

EPROM cell from being erased by ultra- violet light for the normal expected life of an EPROM. Some prior art references taught away from the use of EPROM cells to store redundancy address information in an EPROM.^[13]

At the time of Folmsbee's invention, others did not believe EPROM cells could be used to store redundancy address information. The inventor himself had doubts, as did his supervisor, Mr. Spaw.

ID at 206. The ALJ also found that Atmel did not use this EPROM design until Korsh left Intel and started work at Atmel. During his employment by Intel, Korsh knew of Folmsbee's work and knew that a patent application was pending. Prior to Korsh's arrival, Atmel had tried and failed to design an UPROM, and instead "Atmel relied on inferior polysilicon fuses for storing redundancy address information." ID at 208.

[9] Based on all of these factual findings, none of which are seriously challenged, the Commission concluded, as did the ALJ, that "respondents had failed to prove by clear and convincing evidence that claims 1-4 of the '050 patent are invalid" for obviousness under section 103. Decision at 74-75; see also ID at 209. We agree. While the extension of the sidewalls may seem only a minor advance, it was not an obvious one. The extension of the sidewalls increased the life of an UPROM cell demonstrably, giving it previously unknown practical uses. The evidence shows that the results of extending the sidewalls in the manner disclosed in the '050 patent were surprising. Moreover, Atmel itself failed in its attempt to design a UPROM. See *In re Piasecki*, 745 F.2d 1468, 1475, 223 USPQ 785, 790 (Fed. Cir. 1984) (failure of others to provide a feasible solution to a longstanding problem is probative of non-obviousness). We conclude that the

^[13] A 1982 patent, while teaching the use of a redundancy method similar to that in the '050 patent, assumed that the method could not be used in most EPROMs:

Those skilled in the art will recognize that neither this fuse cell nor the EPROM fuse cell may be used in memory arrays such as EPROMs which have an ultraviolet light erasable window since the application of ultraviolet light through the window will not only erase the information contained in the main memory array but will also erase the redundancy programming which has been implemented in the chip.

U.S. Patent No. 4,546,454, col. 8, lines 38-45. See also ID at 207.

Commission correctly determined that Atmel and GI/M failed to prove that the invention disclosed in the claims of the '050 patent would have been obvious.

2. Infringement of the '050 Patent

[10] Atmel and GI/M also challenge the Commission's finding of infringement, arguing that the Commission improperly construed the claims of the '050 patent.²⁰ Claim interpretation is a question of law and thus subject to *de novo* review in this court. *Hormone Research Found., Inc. v. Genentech, Inc.*, 904 F.2d 1558, 1562, 15 USPQ2d 1039, 1042 (Fed. Cir. 1990); *Loctite Corp. v. Ultraseal Ltd.*, 781 F.2d 861, 866, 228 USPQ 90, 93 (Fed. Cir. 1985). The claims are to be interpreted in light of the claim language, the specification, and the prosecution history. *Hormone Research*, 904 F.2d at 1562, 15 USPQ2d at 1042.

The challenged portion of the claim states: whereby said EPROM cell can be *permanently programmed* so that said redundant elements are always used in place of said defective elements.

(Emphasis added.)

The Commission construed the claim phrase "permanently programmed" to mean "for the useful lifetime of the EPROM part under normal operating conditions."²¹ Decision at 75. Thus, the Commission concluded that "permanent" is a relative term, meaning that the UPROM cell will not be erased during the normal life span of the EPROM. The Commission found infringement of the '050 patent because the shielded cells of the accused EPROMs would not be erased during the normal life span of the accused EPROMs.²²

[11] Atmel and GI/M suggest that the Commission's interpretation employs circular reasoning; if the EPROM becomes useless once the UPROM cells fail, then the UPROM cells will always last for the "useful life" of the EPROM. The parties argue that the term "permanently programmed"

²⁰ Atmel and GI/M do not challenge the finding that their EPROMs infringe the '050 patent's claims as interpreted by the Commission.

²¹ The ALJ read this clause to require that an infringing UPROM cell resist erasure for twenty hours of exposure to ultraviolet light. The Commission held that the twenty-hour figure was improper because it referenced the lifespan of the accused devices.

²² The ALJ found that Intel did not prove infringement by Atmel's 1 megabit design (the 1024k EPROM) because it did not prove how long that part withstands erasure. ID at 227. The Commission did not review this finding, Decision at 74, and Intel does not challenge this holding.

must mean that the UPROM cells will avoid erasure until the EPROM fails due to reasons *other* than erasure of the UPROM. This argument is unconvincing; it would require that the UPROM cells always be at least as reliable as any other portions of the chip. The '050 patent contains no such limitation.

Alternatively, Atmel and GI/M read the "permanently programmed" clause to require that an infringing UPROM cell must tolerate 300 hours of ultraviolet light exposure without erasing. Although the specification of the '050 patent stated that the *goal* of the invention was an UPROM cell that could withstand 300 hours of ultraviolet light exposure, this limitation is not contained in the claims. "Where a specification does not *require* a limitation, that limitation should not be read from the specification into the claims." *Specialty Composites v. Cabot Corp.*, 845 F.2d 981, 987, 6 USPQ2d 1601, 1605 (Fed. Cir. 1988) (*citing Lemelson v. United States*, 752 F.2d 1538, 1551-52, 224 USPQ 526, 534 (Fed. Cir. 1985)) (emphasis in original). The claims of the '050 patent state no minimum life span for its shielded UPROM cells, and one should not be read into the claims. The "permanently programmed" limitation only requires that the shielded UPROM cells remain programmed for the normal life of the EPROM.

The Commission's claim interpretation is the only infringement issue raised on appeal. Accordingly, because we conclude that its interpretation is correct, its finding of infringement must stand.

C. The '394 patent

The '394 patent, entitled "Sensing Amplifier for Floating Gate Memory Devices," issued on September 16, 1980. George Perlegos and Saroj Pathak were the named inventors on the patent, which was assigned to Intel. The '394 patent discloses an EPROM with two specific circuits, one that performs column biasing to limit the voltage swing across an array of memory cells in an EPROM and another that splits the voltage on a dummy cell gate. These circuits are used to increase the speed at which the memory cells can be "read." ID at 149.

The ALJ found that the '394 patent was not proven invalid, and that it was not infringed. The Commission reversed, finding that claim 1 of the '394 patent was invalid for obviousness, and that claim 2 was valid and infringed. Each of the Commission's findings has been challenged in these appeals. The Commission also held that Atmel is prevented from challenging the validity of the '394 patent under the doctrine of assignor estoppel. Intel argues that GI/M, as well

can that the UPROM cells will avoid until the EPROM fails due to re-erasure of the UPROM. This is unconvincing; it would require UPROM cells always be at least as any other portions of the chip. The patent contains no such limitation. Natively, Atmel and GI/M read the "permanently programmed" clause to read that an infringing UPROM cell must last 300 hours of ultraviolet light exposure erasing. Although the specification '050 patent stated that the goal of the invention was an UPROM cell that could last 300 hours of ultraviolet light exposure, the limitation is not contained in the specification. Where a specification does not read limitation, that limitation should not be read into the specification into the *Specialty Composites v. Cabot*, 43 F.2d 981, 987, 6 USPQ2d 1601, 2d Cir. 1988) (citing *Lemelson v. States*, 752 F.2d 1538, 1551-52, 224 26, 534 (Fed. Cir. 1985)) (emphasis added). The claims of the '050 patent minimum life span for its shielded cells, and one should not be read claims. The "permanently programmed" limitation only requires that the UPROM cells remain programmed normal life of the EPROM.

Commission's claim interpretation is infringement issue raised on appeal. Natively, because we conclude that its interpretation is correct, its finding of infringement must stand.

'394 patent

94 patent, entitled "Sensing Amplifying Floating Gate Memory Devices," September 16, 1980. George Perlegos and Saroj Pathak were the named inventors of the patent, which was assigned to GI/M. The '394 patent discloses an EPROM specific circuits, one that performs biasing to limit the voltage swing in an array of memory cells in an array and another that splits the voltage of a memory cell gate. These circuits are designed to increase the speed at which the cells can be "read." ID at 149. L.J. found that the '394 patent was invalid, and that it was not in the public interest. The Commission reversed, finding that the '394 patent was invalid for unobviousness, and that claim 2 was valid. Each of the Commission's decisions has been challenged in these appeals. The Commission also held that Atmel was estopped from challenging the validity of the patent under the doctrine of assignor estoppel. Intel argues that GI/M, as well

as Atmel, is prevented from contesting the validity of the '394 patent by the doctrine of assignor estoppel.

1. Assignor estoppel

Assignor estoppel is an equitable doctrine that prevents a patentee who has assigned the rights to a patent from later contending that what was assigned is a nullity. *Diamond Scientific Co. v. Ambico, Inc.*, 848 F.2d 1220, 1224, 6 USPQ2d 2028, 2030 (Fed. Cir. 1988). The doctrine also bars a similar challenge by any party in privity with the assignor. *Id.*

Intel argued before the ALJ that Atmel could not challenge the validity of the '394 patent because one of the inventors, George Perlegos, a major shareholder and chief executive officer at Atmel, had assigned the patent to Intel. Intel further argued that GI/M was similarly estopped because of the close relationship, discussed below, that George Perlegos and Atmel had with GI/M.

The ALJ concluded that if assignor estoppel were a permissible infringement defense in a Commission proceeding both Atmel and GI/M would be estopped from questioning the patent's validity. The ALJ held, however, that "it is inequitable to use the doctrine of assignor estoppel in any patent case before the Commission." ID at 12. She noted that, if Intel were successful in the Commission action, all products that infringe the '394 patent could be denied entry into the United States, including products made by parties not currently before the Commission. She then reasoned that this potential impact on third parties tipped the scale against applying the doctrine of assignor estoppel. ID at 12. Both Atmel and GI/M were thereafter permitted to challenge the validity of the '394 patent.

[12] On review, the Commission correctly concluded that both statutory and case law required that assignor estoppel be considered and applied in section 337 cases. It based this holding on the language of 19 U.S.C. § 1337(c) (1988) that "[a]ll legal and equitable defenses may be presented in all [section 337] cases," and, by analogy, on this court's decision in *Lannom Mfg. Co. v. United States Int'l Trade Comm'n*, 799 F.2d 1572, 1579, 231 USPQ 32, 37, 4 Fed. Cir. (T) 131, 139 (Fed. Cir. 1986), where we held that the Commission's public interest responsibilities do not give it an independent duty to determine the validity of a patent where no party made such a challenge. Since George Perlegos was estopped from challenging the patent's validity, it was necessary for the Commission to determine whether Atmel or GI/M or both were in privity with George

Perlegos and similarly estopped. The Commission used the following test to determine privity:

whether there is an identity of interests between the persons potentially subject to estoppel with respect to the subject matter . . . sufficient to warrant, in light of the equities of the situation, placing the corporation or other person in the shoes of the assignor/inventor.

Decision at 23.

The Commission determined that Atmel was in privity with George Perlegos and was therefore estopped to challenge the patent's validity,² but that GI/M did not have sufficient contacts with George Perlegos for there to be an "identity of interests." Decision at 25. The Commission, in essence, disregarded the relationship between Atmel and GI/M because it found that Atmel was not George Perlegos' "alter ego." The Commission concluded "we do not believe there is any basis for extending the privity chain in this manner." Decision at 24.

Intel has appealed the Commission's decision that GI/M was not estopped because it was not in privity with George Perlegos. It contends that the Commission's test for privity is unnecessarily narrow. We hold that the Commission erred in failing to apply the doctrine of assignor estoppel to GI/M.³

The doctrine of assignor estoppel is applied "to prevent unfairness and injustice." *Diamond*, 848 F.2d at 1224, 6 USPQ2d at 2030. It is an equitable doctrine

[3] mainly concerned with the balance of the equities between the parties. Those in privity with the assignor partake of that balance; hence, extension of the estoppel to those in privity is justified.

Shamrock Technologies, Inc. v. Medical Sterilization, Inc., 903 F.2d 789, 793, 14 USPQ2d 1728, 1732 (Fed. Cir. 1990) (citations omitted).

[13] In determining whether GI/M was in privity with George Perlegos, all contacts between GI/M and George Perlegos, direct and indirect, must be considered, including the contacts between Atmel and GI/M. We are convinced the Commission improperly limited its analysis to whether the relationship between George Perlegos and GI/M was enough to find that the two were in privity. It did not adequately consider the

² Atmel has not appealed the decision that it was estopped.

³ Because GI/M is estopped to challenge the validity of the '394 patent, we do not consider GI/M's argument that claim 2 of the '394 patent was proven invalid.

part George Perlegos played in creating the joint venture between GI/M and Atmel, under which the two corporations sought to mutually develop EPROM designs and processes.

At the time of the joint development program, George Perlegos owned approximately 40% of Atmel's stock and was the corporation's largest single shareholder. Decision at 23. In his position as president and chief executive officer, he was in charge of Atmel's business and finances. Decision at 23. As part of the Atmel-GI/M agreement, George Perlegos personally indemnified GI/M against patent infringement suits, as he had previously indemnified Atmel in some of its business dealings. ID at 16; Decision at 23. The ALJ found that GI/M would not have agreed to the joint development project without this indemnification. ID at 16. Considering George Perlegos' position at Atmel and the extensive role he played in creating the relationship between Atmel and GI/M, it is apparent that GI/M's dealings with Atmel are also, in substance, dealings with George Perlegos. His ownership and control of Atmel and his personal guarantees to GI/M were crucial to the joint venture between the two corporations.

The evidence further shows that the dealings and relationship between Atmel and GI/M were extensive. Among other things, Atmel transferred many of its EPROM designs and processes to GI/M. Decision at 24-25. The Atmel-GI/M venture led to the creation of some of the allegedly infringing EPROMs which are the subject of this investigation. Decision at 24. As part of the agreement, Atmel promised to devote "100%" of George Perlegos' time to the venture for an entire year. ID at 16. George Perlegos personally went to Korea to find a company to act as a foundry to produce EPROMs for GI/M and selected Hyundai Electronics Industries Co., Ltd. (Hyundai), where GI/M's allegedly infringing chips were eventually made. ID at 17. Interestingly, the agreement with Hyundai even named Atmel as a "subsidiary" of GI/M. ID at 17.

Moreover, there was a financial relationship between the corporations. The ALJ found that "Atmel was completely dependent on [GI/M] for financing," ID at 17, while the Commission noted that GI/M personnel served on Atmel's board of directors and that GI/M owned Atmel stock. Decision at 24. Finally, not only did George Perlegos personally promise to indemnify GI/M, his brother Gust Perlegos, an executive and major shareholder at Atmel, also executed an indemnification in favor of GI/M. ID at 16

In spite of these facts, the Commission concluded that George Perlegos and GI/M did not possess an "identity of interests," and thus GI/M was not estopped. The Commission's test is unduly restrictive for an equitable doctrine.¹² We have said that privity depends on the closeness of the relationship based on a balancing of the equities. As this court stated in *Shamrock Technologies*:

Privity, like the doctrine of assignor estoppel itself, is determined upon a balance of the equities. If an inventor assigns his invention to his employer company A and leaves to join company B, whether B is in privity and thus bound by the doctrine will depend on the equities dictated by the relationship between the inventor and company B in light of the act of infringement. *The closer that relationship, the more the equities will favor applying the doctrine to company B.*

Shamrock Technologies, 903 F.2d at 793, 14 USPQ2d at 1732 (emphasis added).

The Commission based its finding of a lack of privity, in part, on the fact that "there is no evidence in the record to suggest that [GI/M] took part in that agreement in order to avail itself of infringing technology." Decision at 24. While this may be true, such an illicit purpose is not necessary to conclude that there was privity between George Perlegos and GI/M. See *Buckingham Prods. Co. v. McAleer Mfg. Co.*, 108 F.2d 192, 44 USPQ 91 (6th Cir. 1939) (privity existed even though the corporation was not organized for the purpose of making use of the patented formulae). What is significant is whether the ultimate infringer availed itself of the inventor's "knowledge and assistance" to conduct infringement. *Shamrock Technologies*, 903 F.2d at 794, 14 USPQ2d at 1733 (quoting *Mellor v. Carroll*, 141 F. 992, 994 (C.C.D. Mass. 1905) (privity between assignors and others who availed themselves of assignor's knowledge and assistance to conduct infringement)); see also *Climax Lock & Ventilator Co. v. Ajax Hardware Mfg. Co.*, 192 F. 126 (W.D.N.Y. 1911) (privity between companies engaged in joint venture to manufacture and market the infringing product). GI/M unquestionably availed itself of the inventor's, and Atmel's, knowledge and assistance. The allegedly in-

¹² Even under the Commission's restrictive test, a review of all the facts, i.e., considering the joint venture between Atmel and GI/M and the relationship between the inventor and Atmel, as well as the relationship between the inventor and GI/M, indicates a substantial identity of interests.

spite of these facts, the Commission found that George Perlegos and GI/M did not possess an "identity of interests," and GI/M was not estopped. The Commission's test is unduly restrictive for an equitable doctrine.² We have said that privity depends on the closeness of the relationship and on a balancing of the equities. As this Court stated in *Shamrock Technologies*:

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fringing EPROMs were the product of the Atmel-GI/M joint development program, and the services of George Perlegos were an important component of that program from its inception. Further, the indemnity agreement between George Perlegos and GI/M created a significant relationship between them. Such an indemnification agreement, in other cases, has alone been enough to find privity. See *Urbain v. Knapp Bros. Mfg. Co.*, 217 F.2d 810 [103 USPQ 337] (6th Cir. 1954); *Weyerhaeuser Timber Co. v. Boostitch, Inc.*, 178 F. Supp. 757, 760-61 [123 USPQ 493] (D.R.I. 1959). That George Perlegos would take on such a liability demonstrates that he had considerable interest in GI/M's contribution to the joint venture and its production of EPROMs.

In view of (1) Atmel's direct transfer of technology to GI/M, (2) George Perlegos' continuous involvement in the joint development program, (3) George Perlegos' (and his brother's) indemnification of GI/M, and (4) GI/M's financial involvement in Atmel and the joint development program, we must conclude that the balance of the equities requires a finding of privity between GI/M and George Perlegos. As the ALJ noted:

The critical time to determine whether Perlegos was in privity with the other respondents was when Perlegos and the respondents entered into the development agreement. It was at that time that GI/M acquired rights from Atmel and assumed obligations to Atmel, and became subject to any impediments on Atmel's ability to challenge the patents in issue. Atmel clearly was subject to the impediments preventing Perlegos from challenging the patents.

ID at 16.

Because of its privity with George Perlegos and Atmel, GI/M should not have been allowed to challenge the validity of the '394 patent before the Commission. Thus, we affirm the Commission's holding that claim 2 of the '394 patent was not invalid and deny GI/M's appeal of that holding. Further, because of our determination that GI/M was in privity with the inventor and was improperly permitted to contest the validity of the '394 patent, the Commission's holding that claim 1 of the '394 patent is invalid is vacated.

2. Infringement of the '394 patent

The first and second claims in the '394 patent read:

1. An amplifier for sensing the binary state of a first MOS floating gate memory device comprising:

a line coupled to said first device;

a first biasing means coupled to said line for charging said line to a first potential when said first device is in one binary state and for preventing said line from dropping below a second potential when said first device is in its other binary state;

a second floating gate memory device substantially identical to said first device for providing a reference load; a biasing circuit coupled to said second device for biasing said second device at a predetermined level;

a second biasing means coupled to said second device for providing a reference potential; comparator means for comparing potentials, said comparator means coupled to said line and coupled to receive said reference potential; whereby said amplifier senses said binary state of said first device and is quickly able to again sense the binary state of said first device since said line is prevented from discharging by said first biasing means.

2. The amplifier defined by claim 1 wherein said first and second biasing means are substantially identical circuits.

There was no substantive prosecution history of the '394 patent; the claims were allowed as filed. ID at 149.

As previously noted, the invention in the '394 patent is directed to circuitry designed for increasing the speed at which the memory cells of an EPROM can be "read." Typically, a number of memory cells in an EPROM are coupled to a common sensing amplifier through a charged column line. At any given time the column line is coupled to, and attempts to read, a single cell. The column line remains charged if it is coupled to a memory cell which is nonconductive, whereas the column line is discharged if it is coupled to a memory cell which is conductive. The individual binary cells are "read" when the charge on the column line is sensed to determine the state of the cell. The time for each "read cycle" can be decreased by holding the charge on the column line to a relatively small voltage swing. In this way the column line requires less time to be recharged after it is connected to a conductive cell. Accomplishing this desirable effect requires (1) an accurate method of keeping a very narrow swing in voltage on the column line, and (2) a method of testing or sensing the column line for very small changes in voltage.

The '394 patent discloses a circuit for charging the column line to one level (charged state) and for preventing it from dropping below another level (discharged state) when the column line is coupled to a

conductive memory cell. The circuit disclosed in the specification uses two transistors with a specified threshold difference between them to set specific upper and lower voltage swings. ID at 166. As soon as the column line voltage drops from the initial value by 0.1 volt, a transistor provides extra current to the column line, preventing the line from dropping more than another 0.1 volt.

The '394 patent also discloses a second circuit, which is biased at a predetermined level to be used as a reference point. This second line is compared with the column line to determine the binary state of the particular cell to which the latter is coupled. This method of testing the column line is called "balanced sensing." ID at 155. In claim 2 of the '394 patent, substantially identical circuits are on the memory side and on the reference side. The specification showed these circuits to be identical.

The ALJ interpreted the term "first biasing means" narrowly and limited it to the two-transistor method disclosed in the specification. She declined to interpret the claim to allow any equivalent structure to the described biasing means. *Cf.* 35 U.S.C. § 112, paragraph 6 (1988). She further noted that if the claims were construed to cover the column biasing circuits used in the accused EPROMs those claims would read on the column biasing circuits disclosed in a prior art Intel patent, Patent No. 4,094,012 ('012). The ALJ also found that, if the claims were read to encompass any other biasing circuits, the claims would be unenforceable due to Intel's inequitable conduct in not revealing the existence of the '012 patent to the PTO. ID at 173.

The Commission rejected the ALJ's narrow construction of the means-plus-function limitation in claims 1 and 2. Decision at 58. The Commission also concluded that the limitation in claim 2 "that the first and second biasing means are substantially identical circuits" was not taught or suggested in the prior art. Moreover, the Commission held that, because the ALJ did not find that Intel intended to mislead the PTO, inequitable conduct had not been established, *citing Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 876, 9 USPQ2d 1384, 1392 (Fed. Cir. 1988) (partially in banc). Decision at 62. Based on these conclusions, the Commission found that the 27C512 EPROM^{*} literally infringed claim 2 of the '394 patent.

^{*}The parties agree that Atmel's 27C512 EPROM is representative of all the accused EPROMs except the 27C256.

[14] Both GI/M and Atmel challenge the Commission's infringement finding. The determination of literal infringement is a question of fact, *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1269-70, 229 USPQ 805, 811 (Fed. Cir. 1986), as is the determination of equivalent structure under 35 U.S.C. § 112, paragraph 6, *D.M.I., Inc. v. Deere & Co.*, 755 F.2d 1570, 1575, 225 USPQ 236, 239 (Fed. Cir. 1985).

The claims of the '394 patent include means-plus-function limitations. Interpretation of such limitations is governed by 35 U.S.C. § 112, paragraph 6. To meet a means-plus-function limitation literally, an accused device must (1) perform the identical function claimed for the means element, and (2) perform that function using the structure disclosed in the specification or an equivalent structure. *Pennwalt*, 833 F.2d at 934, 4 USPQ2d at 1739; *see also Laitram Corp. v. Rexnord, Inc.*, _____ F.2d _____, _____, 19 USPQ2d 1367, 1369-70 (Fed. Cir. 1991); *Durango Assocs., Inc. v. Reliance, Inc.*, 843 F.2d 1349, 1357, 6 USPQ2d 1290, 1295 (Fed. Cir. 1988). Atmel and GI/M contend that the accused device does not perform the identical function and, in any event, does not have structure that is equivalent to the structure disclosed in the specification of the '394 patent.

a. Consistent with the claim language, the Commission stated that "[t]he function of the first biasing means [of the claims of the '394 patent] is to charge the memory cell column line to a first potential . . . and to prevent that column line from dropping below a second potential" and to "maintain[] the voltage swing across the column line within a small limited range." Decision at 67-68. After considering the 27C512's first biasing means, and expert testimony, the Commission found that the functions of the biasing means specified in the claim and the accused devices were "identical." Decision at 68.

[15] Atmel and GI/M contend that the first biasing means in the allegedly infringing 27C512 EPROM has only one function, *i.e.*, "quieting" the column line after the voltage fluctuates from reading a memory cell. The asserted difference is merely semantic. The 27C512 circuit "quiets" the line by keeping it charged at or near a specific potential, and this is done to prevent the charge on the line from dropping any more than necessary. ID at 176-177. Although the biasing means specified in the claim has an indicated "low" potential, while the 27C512 does not, this distinction is irrelevant. The first biasing means limitation of the claim was not for the purpose of assisting the

both GI/M and Atmel challenge the Commission's infringement finding. The definition of literal infringement is a question of law. *Moleculon Research Corp. v. Atmel Corp.*, 793 F.2d 1261, 1269-70, 229 USPQ 811 (Fed. Cir. 1986), as is the question of equivalent structure under § 112, paragraph 6. *D.M.I., Inc. v. Co.*, 755 F.2d 1570, 1575, 225 USPQ 2d 239 (Fed. Cir. 1985).

Claims of the '394 patent include means-plus-function limitations. Interpretation of such limitations is governed by 35 U.S.C. § 112, paragraph 6. To meet a means-plus-function limitation literally, an accused device must (1) perform the identical function claimed for the means element, and (2) perform that function using the structure disclosed in the specification or an equivalent structure. *Pennwalt*, 833 F.2d at 1739; *see also Laitram Rexnord, Inc.*, 19 USPQ2d 1367, 1369-70 (Fed. Cir. 1988); *Durango Assocs., Inc. v. Reliance Indus., Inc.*, 843 F.2d 1349, 1357, 6 USPQ2d 1290, 1295 (Fed. Cir. 1988). Atmel and GI/M contend that the accused device does not perform the identical function literally, and does not have a structure equivalent to the structure disclosed in the specification of the '394 patent. Consistent with the claim language, the decision stated that "[t]he function of the biasing means [of the claims of the '394 patent] is to charge the memory cell line to a first potential . . . and to keep the column line from dropping beyond potential" and to "maintain[] the voltage swing across the column line within a small limited range." Decision at 1739. After considering the 27C512's first asserted difference, and expert testimony, the court found that the functions of the means specified in the claim and the accused devices were "identical." Decision at 1739.

Atmel and GI/M contend that the means in the allegedly infringing 27C512 EPROM has only one function, "quieting" the column line after it fluctuates from reading a memory cell. The asserted difference is merely setting the 27C512 circuit "quiets" the line when it is charged at or near a specific potential, and this is done to prevent the line from dropping any more. ID at 176-177. Although the means specified in the claim has an "initial" potential, while the 27C512 has a "final" potential, this distinction is irrelevant. The means limitation of the claim is for the purpose of assisting the

column to reach a low potential; it was to limit the decrease in voltage, just as the biasing means on the 27C512 device's circuit limits the decrease in voltage. Atmel and GI/M have failed to show that the Commission's conclusion that the first biasing means limitation reads on the 27C512 EPROM is not supported by substantial evidence. *SSIH*, 718 F.2d at 371-72, 218 USPQ at 684.

b. Next, we consider whether the structure used in accomplishing the biasing function in the 27C512 EPROM is equivalent to the structure described in the specification of the '394 patent. Atmel and GI/M urge that the Commission improperly construed the claims of the '394 patent in view of the specification and the prior art. They argue that a finding of equivalency of structure under section 112, paragraph 6, cannot be made if prior art is considered. To support their argument they cite *Lemelson v. United States*, 752 F.2d 1538, 224 USPQ 526 (Fed. Cir. 1985), *ZMI Corp. v. Cardiac Resuscitator Corp.*, 844 F.2d 1576, 6 USPQ2d 1557 (Fed. Cir. 1988), *Texas Instruments v. United States Int'l Trade Comm'n*, 805 F.2d 1558, 231 USPQ 833, 5 Fed. Cir. (T) 32 (Fed. Cir. 1986), *Loctite*, 781 F.2d 861, 228 USPQ 90, and *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984).

[16] Lemelson, ZMI, ACS, and Loctite are inapposite because they do not involve means-plus-function claim limitations. Clearly, Atmel and GI/M have confused equivalence under the doctrine of equivalents with equivalent structure under section 112, paragraph 6. As this court stated in *D.M.I.*, 755 F.2d at 1575, 225 USPQ at 239:

Thus the word "equivalent" in § 112 should not be confused, as it apparently was here, with the "doctrine of equivalents." In applying the doctrine of equivalents, the fact finder must determine the range of equivalents to which the claimed invention is entitled, in light of the prosecution history, the pioneer-non-pioneer status of the invention, and the prior art. It must then be determined whether the entirety of the accused device or process is so "substantially the same thing, used in substantially the same way, to achieve substantially the same result" as to fall within that range. *Graver Tank & Mfg. Co. v. Linde Air Products Co.*, 339 U.S. 605, 610, 85 USPQ 328, 330 (1950). In applying the "means plus function" paragraph of § 112, however, the sole question is whether the single means in the accused device which performs the function stated in the claim is the same as or an equivalent

of the corresponding structure described in the patentee's specification as performing that function.

See also Data Line Corp. v. Micro Technologies, Inc., 813 F.2d 1196, 1201, 1 USPQ2d 2052, 2055 (Fed. Cir. 1987).

In *Johnston v. Ivac Corp.*, 885 F.2d 1574, 1580, 12 USPQ2d 1382, 1386-87 (Fed. Cir. 1989), this court also noted that section 112, paragraph 6, operates to limit a claim from every possible means to those which are "equivalent."

Properly understood section 112 ¶6 operates more like the reverse doctrine of equivalents than the doctrine of equivalents because it restricts the scope of the literal claim language.

Id. See also Pennwalt, 833 F.2d at 934, 4 USPQ2d at 1739 ("section 112, paragraph 6, rules out the possibility that any and every means which performs the function specified in the claim *literally* satisfies that limitation" (emphasis in original)).

It is not necessary to consider the prior art in applying section 112, paragraph 6. Even if the prior art discloses the same or an equivalent structure, the claim will not be limited in scope thereby. It is only necessary to determine what is an equivalent to the structure disclosed in the specification which is performing the function at issue. When the prior art is considered in the context of the doctrine of equivalents, however, the purpose is to ensure that the patent holder does not obtain a broader right to exclude under that doctrine than could have been obtained from the patent office. *See Wilson Sporting Goods Co. v. David Geoffrey and Assocs.*, 904 F.2d 677, 14 USPQ2d 1942 (Fed. Cir. 1990). Although under the doctrine of equivalents prior art restricts the extent to which patent protection can be equitably extended beyond the claims to cover an accused device, the policies underlying that concept are not served by restricting claim limitations in the same manner. Claim limitations may, and often do, read on the prior art, particularly in combination patents.

That all elements of an invention may have been old (the normal situation), or some old and some new, or all new, is however, simply irrelevant. Virtually all inventions are combinations and virtually all are combinations of old elements.

Environmental Designs, Ltd. v. Union Oil Co., 713 F.2d 693, 698, 218 USPQ 865, 870 (Fed. Cir. 1983).

Thus, under section 112, paragraph 6, the aids for determining a structural equivalent to the structure disclosed in the patent specification are the same as those used in inter-

preting any other type of claim language, namely, the specification, the prosecution history, other claims in the patent, and expert testimony. *See e.g., Symbol Technologies, Inc. v. Opticon Inc.*, 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991); *King Instrument*, 767 F.2d at 862, 226 USPQ at 408; *Palumbo v. Don-Joy Co.*, 762 F.2d 969, 975, 226 USPQ 5, 8 (Fed. Cir. 1985); *cj. McGill Inc. v. John Zink Co.*, 736 F.2d 666, 221 USPQ 944 (Fed. Cir. 1984).

In *Texas Instruments* this court suggested, in dicta, that there might be some similarities between the equivalence analysis under section 112, paragraph 6, and the application of the doctrine of equivalents. *See Texas Instruments*, 805 F.2d at 1569-71, 231 USPQ at 839-41. That case did not suggest, however, that the prior art should be considered in determining literal satisfaction of a means-plus-function claim limitation.

Atmel and GI/M also contend that their means of controlling the voltage level on the column line is not structurally equivalent to that described in the '394 patent. The Commission reversed the ALJ's finding of non-infringement on the grounds that she had improperly limited the "column biasing means" to the precise two-transistor method disclosed in the specification of the '394 patent and did not consider equivalents to that structure.

[17] The broadest definition of a "biasing" circuit is any circuit that places another circuit "in some condition." *Id.* at 184. The 27C512 uses a transistor in conjunction with a negative feedback circuit to limit the voltage swings on the column line. Thus, the accused device clearly has a "biasing" means.

The Commission found:

Both the claimed and the accused circuits use MOS transistors . . . to pull up the column line voltage as it begins to drop and to keep the column line voltage at a minimum level so that the capacitance associated with it does not discharge. *Decision at 69.* The Commission found even less difference between the second biasing means on the claimed and accused devices.

The accused reference cell column biasing circuit differs from the claimed reference cell column biasing circuit only in the sizes and number of the load transistors.

Decision at 69. Finally, the Commission, agreeing with the ALJ, found that the accused device met the limitation in claim 2, *i.e.*, that the first and second biasing circuits in the device are "substantially identical circuits."

Atmel and GI/M offer little to overcome these findings. The main thrust of their argument here mirrors their argument regarding identical function presented above. GI/M, for example, argues "nothing in the accused circuit can establish a second, lower voltage below which the column is prevented from falling" and contends that "the Commission overlooked these clear distinctions." While GI/M's argument points to distinctions that may be clear, the Commission did not find them to be significant. Atmel contends that the first and second biasing circuits on the 27C512 are not substantially similar because the '394 uses a separate biasing circuit to set the "dummy" cell at a voltage lower than that which drives the memory cells, whereas the reference cell on the 27C512 is set to a predetermined level by a separate word line. There was expert testimony offered by both sides on these alleged distinctions, and we cannot say that the Commission's findings were not supported by substantial evidence. Under section 112, paragraph 6, the means used by the accused and claimed devices need not be identical, merely equivalent.

We conclude that the Commission's findings of infringement of claim 2 of the '394 patent must be affirmed.

IV

In Texas Instruments, Inc. v. United States Int'l Trade Comm'n, 871 F.2d 1054, 10 USPQ2d 1257 (Fed. Cir. 1989), we considered whether it was necessary to review the Commission's decision on the validity and infringement of a patent, after the Commission's exclusion order was found to be fully supported by other, more recently issued patents. As in the case before us, the *Texas Instruments* court was considering a limited exclusion order, directed solely at the parties before it. It concluded:

The Commission's exclusion order is directed only to the Samsung DRAM's involved in this litigation and that order is sustainable on the basis of the '701 patent. There is thus no occasion for us to decide the question of infringement of the '764 patent. We shall therefore vacate the Commission's determination that the Samsung DRAMs do not infringe claims 16, 17, and 19 of the latter patent.

Id. at 1067, 10 USPQ2d at 1267. The court also refused to consider the validity and enforceability of another patent since such consideration was unnecessary to support the exclusion order. *Id.* at 1063-64, 10 USPQ2d at 1264. The Commission's determinations

and GI/M offer little to overcome these findings. The main thrust of their argument mirrors their argument regarding the function presented above. GI/M, for example, argues "nothing in the accused can establish a second, lower voltage which the column is prevented from having" and contends that "the Commission has not made these clear distinctions." While this argument points to distinctions that are clear, the Commission did not find them to be significant. Atmel contends that the second biasing circuits on the accused are not substantially similar because it uses a separate biasing circuit to set a "dummy" cell at a voltage lower than that which drives the memory cells, whereas the reference cell on the 27C512 is set to a determined level by a separate word line. This was expert testimony offered by both parties in these alleged distinctions, and we find that the Commission's findings are supported by substantial evidence. Section 112, paragraph 6, the means by which the accused and claimed devices are to be identical, merely equivalent. We conclude that the Commission's finding of infringement of claim 2 of the '394 must be affirmed.

IV

Texas Instruments, Inc. v. United Int'l Trade Comm'n, 871 F.2d 1054, 20 USPQ2d 1257 (Fed. Cir. 1989), we considered whether it was necessary to review the Commission's decision on the validity of the '394 patent, after the Commission's exclusion order was found to be unsupported by other, more recently issued patents. As in the case before us, the *Texas Instruments* court was considering a Commission's exclusion order, directed solely at the '394 patent. It concluded:

The Commission's exclusion order is directed only to the Samsung DRAM's involved in this litigation and that order is sustainable on the basis of the '701 patent. There is thus no occasion for us to decide the question of infringement of the '764 patent. We shall therefore vacate the Commission's determination that the Samsung DRAMs do not infringe claims 17, and 19 of the latter patent. 1067, 10 USPQ2d at 1267. The court refused to consider the validity and enforceability of another patent since such consideration was unnecessary to support the exclusion order. *Id.* at 1063-64, 10 USPQ2d at 1267. The Commission's determinations

relating to these issues were therefore vacated. *Id.*¹⁸

[18] Following the teaching of *Texas Instruments*, we have considered the questions involving the most recently issued Intel patents in the reverse order of their issue dates. The issues resolved above fully support the scope and duration of the Commission's exclusion order and its cease and desist orders against Atmel and GI/M. We therefore do not need to consider the remaining infringement and validity issues presented by the parties in the three consolidated appeals. Accordingly, we vacate the remaining portions of the Commission's determinations that have been appealed.

To summarize our conclusions:

In Atmel's appeal, No. 89-1476, the Commission's determination that the Intel-Sanyo agreement did not cover Atmel's EPROMs is affirmed. The Commission's determinations that Atmel's "old" 51 Series EPROMs infringed the '084 patent, its 64K, 512K, and 256K EPROMs infringed the '050 patent, its 64K, 51 Series, and 1024K EPROMs infringed claim 2 of the '394 patent, and that those patents were not proven invalid, are also affirmed. The Commission's exclusion and cease and desist orders are affirmed to the extent consistent with our determinations.

In GI/M's appeal, No. 89-1534, the Commission's determination that GI/M's "old" 51 Series EPROMs infringed the '084 patent, its 256K and 51 Series infringed the '050 patent, and its 51 Series infringed claim 2 of the '394 patent, and that those patents had not been proven invalid, are affirmed. We reverse the Commission's conclusion that GI/M was not estopped from challenging the '394 patent's validity. The Commission's determinations that GI/M has not proven the '189 patent invalid and that GI/M infringed that patent are vacated. The Commission's orders with respect to GI/M are modified by deleting references to the '189 patent and are otherwise affirmed to the extent consistent with our determinations.

¹⁸ But see *SSIH Equip. S.A. v. United States Int'l Trade Comm'n*, 718 F.2d 365, 370 n.8, 218 USPQ 678, 683-84 n. 8, 1 Fed. Cir. (T) 90, 94 n.8 (Fed. Cir. 1983), where this court stated, in dictum, that "[b]y practice, the Commission issues exclusion orders covering several independent bases for exclusion of goods rather than separate exclusion orders for each. The multiple based approach was taken here in that goods infringing any one of the claims were excluded. Thus, in practical effect, the June 19 order may be thought of as separate orders on each claim." (Emphasis in original).

In Intel's appeal, No. 89-1459, we vacate the Commission's determination that claim 1 of the '394 patent is invalid. We also vacate the Commission's determinations that neither Atmel nor GI/M infringed the '255 and '108 patents. Intel's appeal of these Commission determinations is dismissed.

COSTS

Each party shall bear its own costs.

AFFIRMED-IN-PART, REVERSED-IN-PART, AND VACATED-IN-PART

District Court, S.D. New York

Childress v. Taylor

No. 87 Civ. 6924 (CSH)

Decided November 27, 1990 and February 22, 1991

COPYRIGHTS

1. Elements of copyright — Statutory elements — Originality (§205.0707)

Rights in copyright; infringement — Ownership of copyright — Joint works (§213.0303)

Individual who gave playwright idea for writing play about life of "Moms" Mabley, who conducted research into factual aspects of Mabley's life and career, who made that research available to playwright, and who perceived herself as co-author, is not thereby entitled to designation of play as joint work pursuant to 17 USC 101, since copyright law does not protect research and facts are not copyrightable, since individual's creative suggestions concerning play fall far short of "substantial and significant contribution" required to reach finding of joint ownership, and since individual's state of mind regarding co-authorship was not shared by playwright.

2. Rights in copyright; infringement — Right to reproduction — Access, copying, and substantial similarity — Works similar (§213.0503.03)

TRADEMARKS AND UNFAIR TRADE PRACTICES

Infringement; conflicts between marks — Passing off (§335.07)

Defendants' play, "Moms: The First Lady of Comedy," about life of black comedienne